

Simulation of Electrical Characteristics of Gate All around Silicon Nanowire Field Effect Transistor using Extended Hückel Theory Based Semi Empirical Approach

Mayank Chakraverty¹, Harisankar P S², Vaibhav Ruparelia³

^{1, 2, 3}(RF Analog & Mixed Signal PDK Enablement, GLOBALFOUNDRIES, Bangalore, India)

ABSTRACT : Gate All Around (GAA) FET stands out as one of the most promising FET designs to replace the currently planar MOSFETs due to its ability to provide better gate control and better immunity to short channel effects. This paper reports the electrical characteristics of GAA Silicon Nanowire Field Effect Transistor obtained using Extended Huckel Theory based Semi Empirical Method. The physics behind the Semi Empirical method has been presented in brief. The nanowire transistor has been simulated with two different gate dielectrics (SiO_2 & ZrO_2) and the electrical characteristics resulting from the two structures have been compared for power efficiency. A comparison of off-state current and off-state channel conductance between the two nanowire transistor structures has been presented towards the end of the paper that demonstrates that ZrO_2 gate dielectric based silicon nanowire transistor is power efficient than its counterpart with SiO_2 gate dielectric..

Keywords – Gate All Around, MOSFETs, Semi Empirical, Extended Hückel, Nanowire, Gate Dielectric

I. INTRODUCTION

Nanowire (NW) FETs have been proposed and now studied by many research groups around the world. This is because, they are promising candidate to sustain the relentless progress in scaling of CMOS devices [1] [3]. Several key factors have contributed to the boom in NW research. First, semiconductor NWs can be prepared in high-yield with reproducible electronic properties as required for Very Large Scale integrated (VLSI) systems. Second, compared with “top-down” nanofabricated device structures, “bottom-up” synthesized NW materials offer well controlled size; that is at or beyond the limits of lithography. In addition, the crystalline structures, smooth surfaces and the ability to produce radial and axial NW hetero structures can reduce scattering. These results in higher carrier mobility when compared with nanofabricated samples with similar size. Finally, the body thickness (diameter) of NWs can be controlled down to well below 10 nm. Therefore, electrical integrity of NW-based electronics can be maintained even as the gate length is aggressively downscaled. This is a feature that has become increasingly difficult to achieve in conventional MOSFETs [3]. Gate All Around (GAA) SiNW FETs have attracted significant interest because of their excellent electrostatic integrity even at the nanoscale [8]. Various types of SiNW FETs are being explored as a promising candidate for future transistors replacing planar MOSFETs in logic and Dynamic Random Access Memory (DRAM) applications, and their fabrication is being studied either from top-down or bottom-up approaches [2] [7]. Since silicon planar MOSFETs are approaching their scaling limits, new device designs are being explored to replace the existing planar technology. Among the possible new device designs are Double Gate (DG) FETs, FinFETs, Tri-Gate FETs and Omega- Gate FETs. The Silicon Nanowire GAA FET stands out as one of the most promising FET designs to replace the currently planar MOSFETs due to its ability to provide better gate control and better short channel performance [6]. Recent developments such as synthesis of highly ordered nanowires and fabrication of nanowires as small as 1nm in diameter have illustrated the progress possible in silicon nanowire technology. Silicon nanowire devices exhibit higher transconductance and more ideal sub threshold behavior with improved on-current, reduced off-current and lower sub threshold slope [9].

II. EXTENDED HÜCKEL THEORY BASED SEMI EMPIRICAL APPROACH

The simulations carried out in this paper use ATK-Semi Empirical (ATK-SE) formalism. This ATK-SE formalism uses the Semi Empirical Extended Hückel model to calculate the transmission characteristics of the nanowire. The extended Hückel method is a semi empirical quantum chemistry method, developed by Roald Hoffmann since 1963. It is based on the Hückel method but, while the original Hückel method only considers pi

orbitals, the extended method also includes the sigma orbitals. The extended Hückel method can be used for determining the molecular orbitals, but it is not very successful in determining the structural geometry of an organic molecule. It can however determine the relative energy of different geometrical configurations. It involves calculations of the electronic interactions in a rather simple way for which the electron-electron repulsions are not explicitly included and the total energy is just a sum of terms for each electron in the molecule. In the extended Hückel method, only valence electrons are considered; the core electron energies and functions are supposed to be more or less constant between atoms of the same type. The method uses a series of parametrized energies calculated from atomic ionization potentials or theoretical methods to fill the diagonal of the Fock matrix. After filling the non-diagonal elements and diagonalizing the resulting Fock matrix, the energies (eigenvalues) and wave functions (eigenvectors) of the valence orbitals are found. The ATK-SE formalism can model the electronic properties of molecules, crystals and devices using both self-consistent and non-self-consistent tight-binding models [4]. In ATK-SE, the non-self-consistent part of the tight-binding Hamiltonian is parametrized using a two-center approximation, i.e. the matrix elements only depend on the distance between two atoms and is independent of the position of the other atoms. In the extended Hückel model, the matrix elements are described in terms of overlaps between Slater orbitals on each site. In this way, the matrix elements can be defined by very few parameters [5]. In the Slater-Koster model, the distance-dependence of the matrix elements is given as a numerical function; this gives higher flexibility, but also makes the fitting procedure more difficult. The self-consistent part of the calculation is identical for both SE models. The density matrix is calculated from the Hamiltonian using non-equilibrium Green's functions (NEGF) for device systems, while for molecules and crystals it is calculated by diagonalization. The density matrix defines the real-space electron density, and consequently the Hartree potential can be obtained by solving the Poisson equation [4] [5].

III. SIMULATION SET UP

In this paper, a silicon nanowire transistor structure has been built and simulated in two sets - once with SiO₂ as gate dielectric and next with ZrO₂ as gate dielectric. The nanowire transistor simulated has a silicon nanowire oriented in (100) direction. The nanowire is essentially a single crystal structure in Face Centered Cubic orientation. The two ends of the nanowire are doped to obtain a doping concentration of $4 \times 10^9 \text{ cm}^{-3}$ in the source and drain regions, as the electrode is about 1 nm long and has a cross section of (0.5 nm)X(0.5 nm). As the nanowire transistor simulated has a Gate All Around structure that offers better control over the carriers in the channel, the gate dielectric layer and the metal gate are essentially cylindrical in shape to wrap over the silicon nanowire, unlike conventional planar MOSFETs where the gate dielectric and the metal gate are just material stacks sitting over the channel area on the substrate. The thickness of the gate dielectric used in this device design is 2 Å while the inner radius is 5 Å. The thickness of the metal gate is 3 Å while the inner radius is 7 Å. The thickness and inner radii of the layers have been deliberately kept the same in the two structures of the GAA nanowire FET so that it is convenient to compare the characteristics of both the structures which differ in terms of the gate dielectric material. The schematic of the simulated device is shown in Fig. 1 (right).

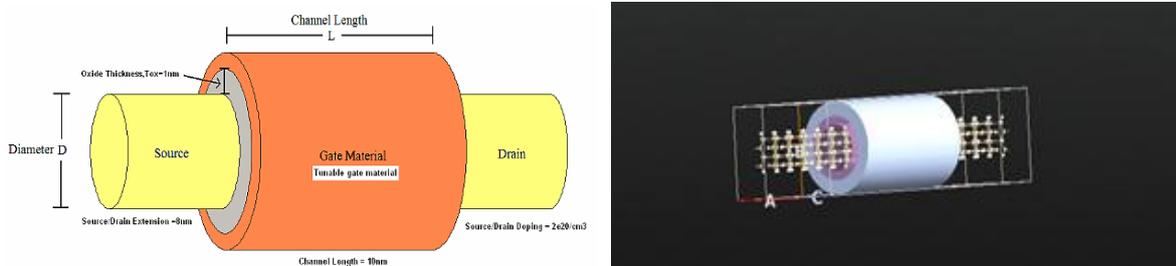


Fig.1. Schematic of GAA NWFET (Left) and Simulated GAA NWFET structure (Right)

IV. SIMULATION RESULTS AND ANALYSIS WITH SILICON DIOXIDE GATE DIELECTRIC

Once the simulation settings are set, iterative simulations have been performed in such a way that for a gate bias of 0 V, drain voltage is swept from 0 V to 2 V in steps of 0.2 V. For each value of drain voltage, a single simulation is run followed by the subsequent simulation with a different drain voltage. Once the drain voltage is swept from 0 V to 2 V for gate bias of 0V, the gate voltage is changed to 0.5 V and simulations have been carried out for different values of drain voltages. In this way, the nanowire field effect transistor has been simulated for gate bias of 0 V to 2.5 V in steps of 0.5 V, drain voltage being swept from 0 V to 2 V for each gate voltage set. For a particular gate voltage, simulation result gives the I-V curve obtained by sweeping the drain voltage from 0 V to 2 V.

Once the electrical characteristics have been obtained for the NWFET for six different gate voltages, the values of current have been extracted from each I-V curve for each value of drain voltage and gate voltage. Using the extracted data, the transfer characteristics and the drain characteristics have been plotted, as shown in Fig. 2.

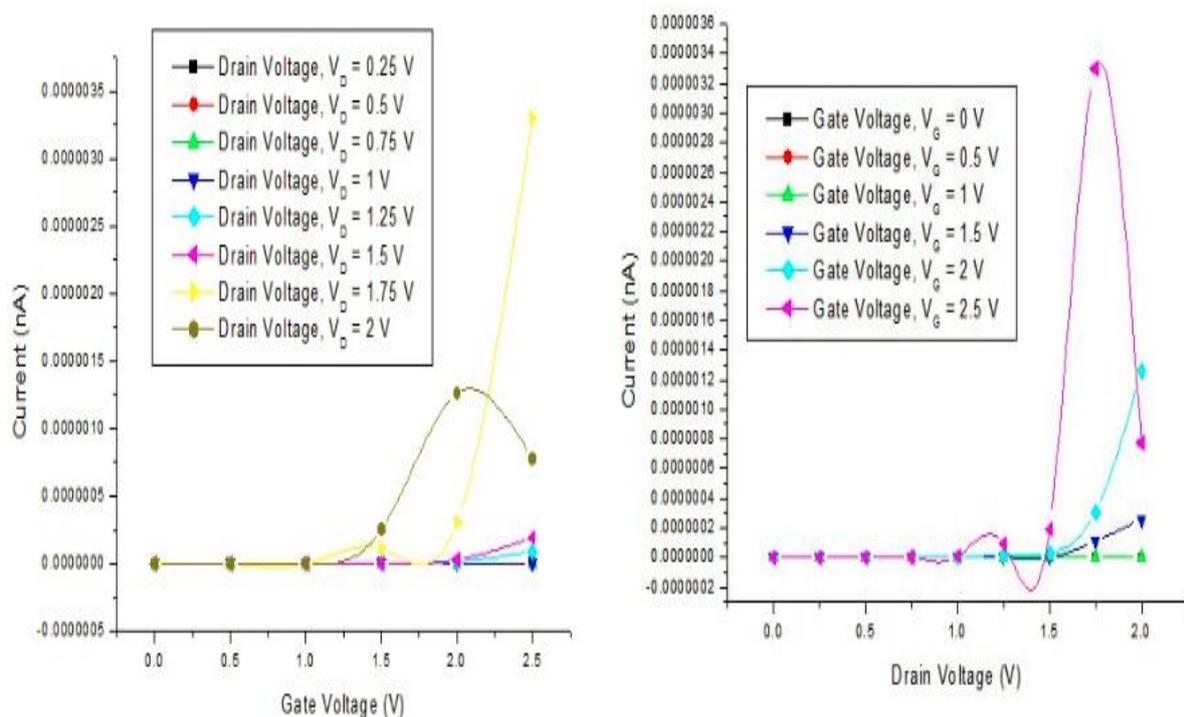


Fig.2. Transfer Characteristics & Drain Characteristics of Silicon NWFET with SiO₂ Gate Dielectric

In Fig. 2, the drain current has been plotted against gate voltage for different values of drain voltage. The threshold voltage, V_{TH} of the NWFET is equal to 0.21 V.

The channel conductance has been computed for different gate voltages used for the simulations. Fig. 3 (left) depicts the plot of channel conductance plotted against the corresponding gate voltages applied. A similar curve can be obtained by plotting the conductance values against drain voltages applied for different gate voltage values as depicted in Fig. 3 (right). As it is evident from the two plots, the channel conductance is low for low values of gate and drain voltages in both the plots. As the voltages are increased, the channel conductance shoots up and is highest for $V_G = 2.5$ V and $V_D = 2$ V. Also, from Fig. 5.1, negative resistance regions are evident in a couple of plots, which implies that for the voltage values specified in those plots, the NWFET can be used for microwave applications.

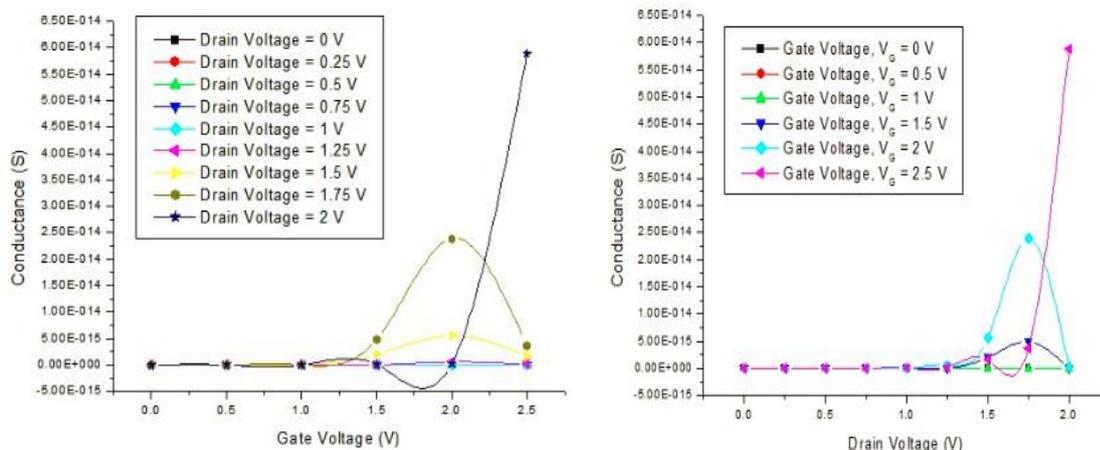


Fig.3. Conductance plotted against Gate Voltage (left) and Drain Voltage (right)

V. TEMPERATURE DEPENDENCE OF CHANNEL CONDUCTANCE WITH SiO₂ GATE DIELECTRIC

For operating temperatures of 0 K, 77 K, 300 K and 325 K, the NWFET with SiO₂ gate dielectric has been simulated for a gate bias of $V_{TH} = 0.21$ V. It can be observed from the plot in Fig. 4 (left) that the channel conductance shoots up at room temperature, ensuring that the device with SiO₂ gate dielectric is well suited to operate at room temperature. Whereas, the conductance is low at other operating temperatures.

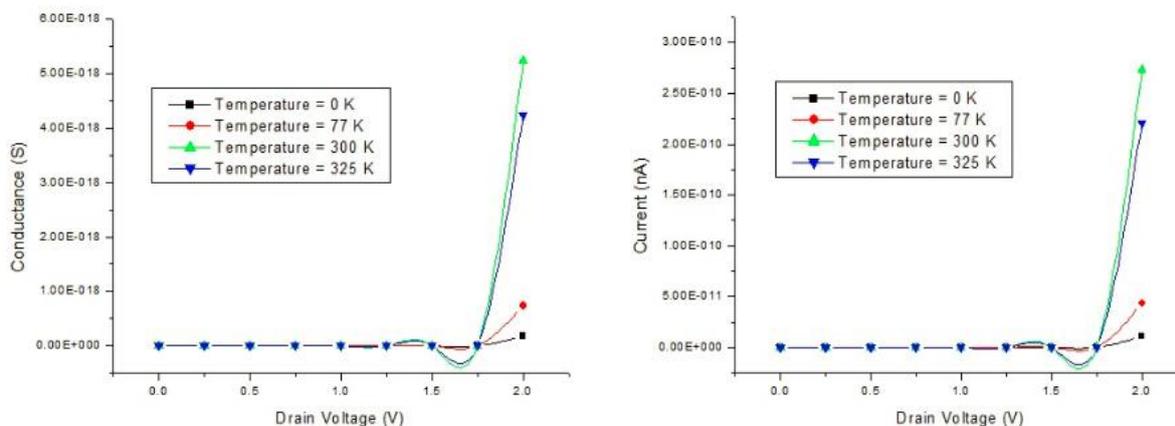


Fig. 4. Temperature Dependence of Channel Conductance with Variation in Drain Voltage at $V_G = 0.21$ V (left) and $V_G = V_{TH}$ (right)

The Fig. 4 (right) depicts the temperature dependence of drain current with a variation in drain voltage for a gate voltage, $V_G = V_{TH}$. As evident from the plot above, the drain current shoots up at room temperature, ensuring that the device with SiO₂ gate dielectric is well suited to operate at room temperature. Where as, the current is low at other operating temperatures. Therefore, room temperature operation promises higher drive current than other operating temperatures. But when it comes to low drive current leading to lower power dissipation, the silicon NWFET can be operated at lower temperatures.

VI. SIMULATION RESULTS AND ANALYSIS WITH ZIRCONIUM DIOXIDE GATE DIELECTRIC

The steps involved in setting up the simulation for ZrO₂ gate dielectric based nanowire FET is similar to the set up with SiO₂ gate dielectric, except that while entering the dielectric constant of the gate dielectric, the value to be entered is 25. Rests of all the steps remain the same. Once the device structure is set up with just a single change with respect to the gate dielectric constant value being equal to 25 instead of 3.9, iterative simulations have been performed in a similar way as done for the NWFET with SiO₂ gate dielectric.

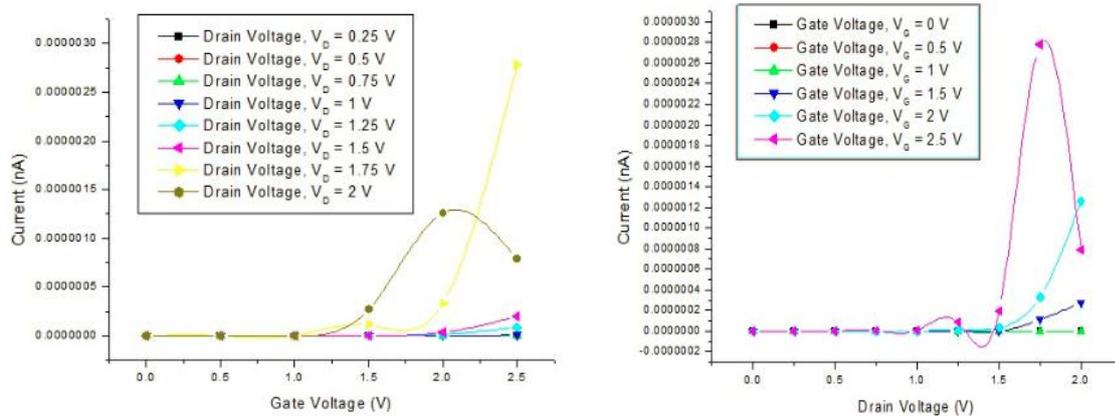


Fig.5. Transfer and Drain Characteristics of Silicon NWFET with ZrO_2 Gate Dielectric

For a particular gate voltage, simulation result gives the I-V curve obtained by sweeping the drain voltage from 0 V to 2 V. It is seen that the I-V plots thus obtained are very similar in terms of the current values and the features observed. This is because the entire device structure remains the same as used with SiO_2 gate dielectric, the only change is the dielectric constant. Once the electrical characteristics have been obtained for the NWFET for six different gate voltages, the values of current have been extracted from each I-V curve for each value of drain voltage and gate voltage. Using the extracted data, the transfer characteristics and the drain characteristics have been plotted, as shown in Fig. 5. The drain current has been plotted against gate voltage for different values of drain voltage in Fig. 5. The threshold voltage, V_{TH} of the NWFET is equal to 0.17 V.

As done in case of NWFET with silicon dioxide as gate dielectric in the previous section, the channel conductance has been computed for different gate voltages used for the simulation. Fig. 6 (left) depicts the plot of channel conductance plotted against the corresponding gate voltages applied. A similar curve can be obtained by plotting the conductance values against drain voltages applied for different gate voltage values as depicted in Fig. 6 (right). As it is evident from the two plots, the channel conductance is low for low values of gate and drain voltages in both the plots. As the voltages are increased, the channel conductance shoots up and is highest for $V_G = 2.5$ V and $V_D = 2$ V. Also, from Fig. 5 & 6, negative resistance regions are evident in a couple of plots, which implies that for the voltage values specified in those plots, the NWFET can be used for microwave applications.

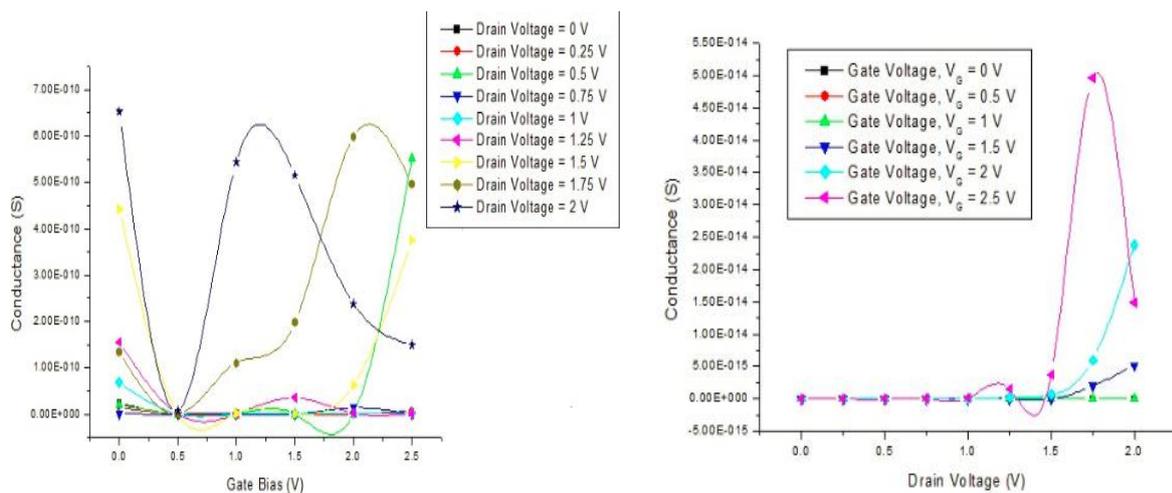


Fig. 6. Conductance plotted against Gate Voltage (left); and Drain Voltage (right)

It can be seen from the transfer and drain characteristics of the silicon NWFET using SiO_2 and ZrO_2 as dielectrics respectively, the current values are slightly less in case of NWFET with ZrO_2 as gate dielectric.

Moreover, due to higher dielectric constant ($25 > 3.9$), the gate leakage current is obstructed to a much larger extent in case of ZrO_2 than in NWFET with SiO_2 gate dielectric. This leads to much lower power consumption in case of ZrO_2 gate dielectric based NWFET as compared to SiO_2 gate dielectric based NWFET.

VII. COMPARISON OF SILICON DIOXIDE AND ZIRCONIUM DIOXIDE BASED SILICON NWFET

From the transfer and drain characteristics of the NWFET with SiO_2 gate dielectric and ZrO_2 gate dielectric respectively, it is evident that the power consumption is more in case of Silicon NWFET with SiO_2 gate dielectric owing to gate leakage current, as discussed in the previous section. Also, the comparisons of the off state drain current in the two devices as plotted against the drain voltages with different gate dielectrics have been presented in Fig. 7 (left). It is clear from the plot that the off state drain current is slightly higher in case of silicon NWFET with SiO_2 gate dielectric as compared to the NWFET with ZrO_2 gate dielectric.

Similar to the plot above, the channel conductance can be plotted against the drain voltages for the two NWFETs with SiO_2 and ZrO_2 gate dielectrics respectively, as shown in Fig. 7 (right). As seen in Fig. 7, the off state channel conductance is slightly higher in case of silicon NWFET with SiO_2 gate dielectric as compared to the NWFET with ZrO_2 gate dielectric. This comparison adds to the performance metrics of silicon NWFET with ZrO_2 as gate dielectric, owing to its lower power consumption and obstruction to short channel effects owing to higher dielectric constant of ZrO_2 .

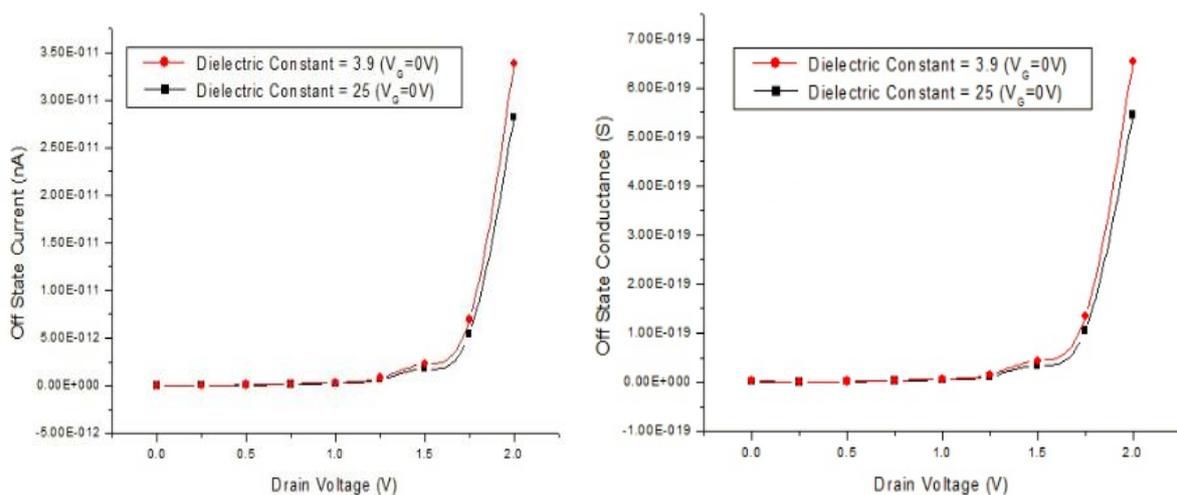


Fig.7. Comparison of off state drain current and off state channel conductance of Si NWFET with SiO_2 gate dielectric against ZrO_2 gate dielectric

VIII. CONCLUSION

In this paper, an investigation of the electrical characteristics of an n-channel Silicon Nanowire Field Effect Transistor obtained using Extended Hückel Theory (EHT) based Semi Empirical (SE) Approach has been carried out. Using the EHT based SE approach, the nanowire transistor has been simulated with two different gate dielectrics, silicon dioxide and zirconium dioxide. The resulting electrical characteristics have been compared for power efficiency. A study of the temperature dependence of the electrical characteristics of the silicon nanowire transistor has been performed based on simulation with temperature variation. A comparison of the off-state drain current and off-state channel conductance of the nanowire device with silicon dioxide and zirconium dioxide has been presented towards the end of the paper. To conclude, the nanowire transistor with zirconium dioxide as gate dielectric is seen to offer better power performance as compared to the nanowire device with silicon dioxide gate dielectric. Further work could be done by simulating nanowire FET with new materials such as SiGe nanowire channel, compound semiconductor nanowire channel with other high-k dielectrics.

REFERENCES

- [1] Mayank Chakraverty et al., Simulation of Electrical Characteristics of Silicon and Germanium Nanowires Progressively Doped to Zener Diode Configurations using First Principle Calculations, *Lecture Notes in Electrical Engineering*, Volume 372, 2015, 421-428.
- [2] Chakraverty Mayank, Gupta Kinshuk, Babu Vinay G. et al., A Technological Review on Quantum Ballistic Transport Model Based Silicon Nanowire Field Effect Transistors for Circuit Simulation and Design, *Journal of Nanoscience, Nanoengineering and Applications*. 5(2), 2015, 20–31.
- [3] Ali Razavieh et al., Effect of Diameter Variation on Electrical Characteristics of Schottky Barrier Indium Arsenide Nanowire Field Effect Transistors, *ACS Nano*, 8 (6), 2014, 6281–6287.
- [4] R. G. Parr and W. Yang, *Density-functional theory of atoms and molecules*, Oxford Univ. Press, 1994, ISBN 978-0195092769.
- [5] W. Kohn and L. J. Sham, Self-consistent equations including exchange and correlation effects, *Phys. Rev.*, vol. 140, no. 4 A, 1965, A1133–A1138.
- [6] A. Chaudhry, J.N. Roy, MOSFET Models, Quantum Mechanical Effects and Modeling Approaches: A Review, *Semiconductor Technol. Sci.* 10(1), 2010, 20–27.
- [7] Ahmet Bindal and Sotoudeh Hamedi-Hagh, *Silicon Nanowire Transistors*, Springer International Publishing, ISBN: 978-3-319-27175-0 (Print) 978-3-319-27177-4 (Online), 2016
- [8] A. Marchi, E. Gnani, S. Reggiani, M. Rudan, G. Baccarani, Investigating the performance limits of silicon-nanowire and carbon-nanotube FETs, *Solid-State Electronics*, Volume 50, Issue 1, pp. 78-85, January 2006.
- [9] Y. Cui , Z. Zhong , D. Wang , W. U. Wang and C. M. Lieber, High performance silicon nanowire field effect transistors, *Nano Lett.*, vol. 3, pp. 149-152, 2003.